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Approved for use through 07/31/2006. OMB 0651-0031 U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number. **Application Number** 10/708,056 Filing Date February 5, 2004 TRANSMITTAL First Named Inventor Edmund M. Clarke **FORM** Group Art Unit 3618 (to be used for all correspondence after initial filing) **Examiner Name** Attorney Docket Number 361007-000031 Total Number of Pages in This Submission ENCLOSURES (check all that apply) Fee Transmittal Form Drawing(s) After Allowance Communication to Group Fee Attached Licensing-related Papers Appeal Communication to Board Petition of Appeals and Interferences Amendment / Reply Petition to Convert to a Appeal Communication to Group After Final **Provisional Application** (Appeal Notice, Brief, Reply Brief) Affidavits/declaration(s) Power of Attorney, Revocation Proprietary Information Change of Correspondence **Extension of Time Request** Status Letter Address **Express Abandonment Request** Other Enclosure(s) (please Terminal Disclaimer Information Disclosure Statement identify below): Request for Refund *Acknowledgement Postcard Certified Copy of Priority CD, Number of CD(s) _ *19 cited references **Documents** Response to Missing Parts/ Incomplete Application Remarks Response to Missing Parts under 37 CFR 1.52 or 1.53 SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT CHARLES L. MOORE (REG. NO. 33,742) Individual Name **MOORE & VAN ALLEN** Signature Date July 13, 2004 **CERTIFICATE OF TRANSMISSION/MAILING** I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below. Typed or printed name Katie M. Efland

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date

July 13, 2004

Signature

Attorney Docket: 361007-000031



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Edmund M. Clarke

Group Art Unit:

Serial Number: 10/708,056

Examiner:

Filed: February 5, 2004

For: METHOD AND SYSTEM TO VERIFY A CIRCUIT DESIGN

Commissioner for Patents PO Box 1450 Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.56 AND 37 C.F.R. § 1.97

It is respectfully requested that the documents listed on the attached Form PTO/SB/08A be considered by the Patent and Trademark Office in the above-referenced application and made of record therein. A full text copy of the relevant documents are enclosed. This information disclosure statement submitted herewith is being filed within three months of the filing date of the application or date of entry into the national stage of an international application or before the mailing date of a first Office action on the merits, whichever event occurs last.

Respectfully submitted,

By:

Charles L. Moore

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July 13, 2004

Date

CERTIFICATE OF MAILING

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Complete if Known e for form 1449A/PTO 10/708,056 **Application Number** INFORMATION DISCLOSURE Filing Date February 5, 2004 STATEMENT BY APPLICANT First Named Inventor Edmund M. Clarke Art Unit **Examiner Name** (use as many sheets as necessary) 3 Attorney Docket Number 361007-000031 Sheet

	U.S. PATENT DOCUMENTS							
Examiner Initials'	Cite No. ¹	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear			
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	FOREIGN PATENT DOCUMENTS								
Examiner Initials'	Cite No. ¹	Foreign Patent Document Country Code ³ –Number ⁴ –Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T6			

Examiner	Date	
Signature	Considered	

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					Complete if Known		
Substitute for form 1449B/PTO				Application Number	10/708,056		
	INFORMATION DISCL	osi	JRE	Filing Date	February 5, 2004		
	STATEMENT BY APP			First Named Inventor	Edmund M. Clarke		
				Art Unit			
	(use as many sheets as neo	cessai	y)	Examiner Name			
Sheet	2	of	3	Attorney Docket Number	361007-000031		

		NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Include name of the author (in CAPITA) I ETTERS) title of the article (when appropriate) title of the item				
	В	Carl Pixley, Guest Editor's Introduction: Formal Verification of Commercial Integrated Circuits. IEEE Design & Test of Computers, 18(4):4-5, 2001.			
,	С	Armin Biere, Alessandro Cimatti, Edmund M. Clarke, and Yunshan Yhu. Symbolic model checking without BDDs. In Tools and Algorithms for Construction and Analysis of Systems, pages 193-207, 1999.			
	D	A. Biere, E. Clarke, R. Raimi, and Y. Zhu. Verifying safety properties of a Power PC TM microprocessor using symbolic model checking without BDDs. In N. Halbwachs and D. Peled, editors, Proceedings of the 11 th International Conference on Computer Aided Verification (CAB 99), Lecture Notes in Computer Science. Springer Verlag, 1999.			
	E	A. Biere, A.Cimatti, E.M. Clarke, M. Fujita, and Y. Zhu. Symbolic model checking using SAT procedures instead of BDDs. In Design Automation Conference (DAC '99), 1999.			
	F	Joao P. Marques-Silva and Karem A. Sakallah. GRASP – A New Search Algorithm for Satisfiability. In Proceedings of IEEE/ACM International Conference on Computer-Aided Design, pages 220-227, November 1996.			
-	G	Matthew W. Moskewicz, Conor F. Madigan, Ying Zhao, Lintao Zhang, and Sharad Malik. Chaff: Engineering an efficient SAT solver. In Proceedings of the 38 th Design Automation Conference (DAC '01), June 2001.			
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	1	O. Shtrichman. Tuning SAT checkers for bounded model checking. In E.A. Emerson and A.P. Sistla, editors, Proceedings of the 12 th International Conference on Computer Aided Verification (CAV 2000), Lecture Notes in Computer Science. Springer Verlag, 2000.			
	J	Fady Copty, Limor Fix, Ranan Fraer, Enrico Giunchiglia, Gila Kamhi, Armando Tacchella, and Moshe Y. Vardi. Benefits of bounded model checking at an industrial setting. In Gerard Berry, Hubert Comon, and Alain Finkel, editors, Proceedings of the 13 th International Conference on Computer Aided Verification (CAV 2001), number 2102 in Lecture Notes in Computer Science, pages 436-453. Springer Verlag, 2001.	·		
	Κ.	Per Bjesse, Tim Leonard, and Abdel Mokkedem. Finding bugs in an Alpha microprocessor using satisfiability solvers. In Gerard Berry, Hubert Comon, and Alain Finkel, editors, Proceedings of the 13 th International Conference on Computer Aided Verification (CAV 2001), number 2102 in Lecture Notes in Computer Science, pages 454-464. Springer Verlad, 2001.			

Examiner	Date	•
Signature	Considered	

^{*}EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Applicant's unique citation designation number (optional). Applicant is to place a check mark here if English language Translation is attached.

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				Complete if Known		
Substitute for form 1449B/PTO				Application Number	10/708,056	
	INFORMATION DISCI	osi	JRE	Filing Date	February 5, 2004	
STATEMENT BY APPLICANT				First Named Inventor	Edmund M. Clarke	
				Art Unit		
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Sheet	3	of	3	Attorney Docket Number	361007-000031	

		NON PATENT LITERATURE DOCUMENTS						
Examiner Initials*	Cite No. ¹							
	L	Luc Semeria, Andrew Seawright, Renu Mehra, Daniel Ng, Arjuna Ekanayake, and Barry Pangrle. RTL C-based methodology for designing and verifying a multi-threaded processor. In Proc. Of the 39 th Design Automation Conference ACM Press, 2002.						
	М	I. Page. Constructing Hardware-Software Systems from a Single Description. Journal of VLSI Signal Processing, 1291):87-107, 1996.						
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,	Р	David W. Currie, Alan J. Hu, and Sreeranga Rajan. Automatic formal verification of dsp software. In Proceedings of the 37 th Design Automation Conference (DAC 2000), pages 130-135. ACM Press, 2000.						
	Q	Kiyoharu Hamaguchi. Symbolic simulation heuristics for high-level design descriptions with uninterpreted functions. In International Workshop on High-Level Design, Validation, and Test, pages 25-30. IEEE, 2001.						
	R	C. Blank, H. Eveking, J. Levihn, and G. Ritter. Symbolic simulation techniques – state of the art and applications. In International Workshop on High-Level Design, Validation, and Test, pages 45-50. IEEE, 2001.						
	S	Apt., Krzysztof R. Logics and Models of Concurrent Systems, NATO ASI Series, Series F: Computer and System Sciences, Vol. 13.						

Signature Considered I	Examiner	Date	
	Signature	Considered	

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